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**RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE REQUESTED
EXAMINING GROUP 2123**

PATENT

Customer No. 22,852

Attorney Docket No. 04173.0441

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Hisashi Kaneko et al.

Application No.: 10/757,415

Filed: January 15, 2004

For: SIMULATION CIRCUIT
PATTERN EVALUATION
METHOD, MANUFACTURING
METHOD OF SEMICONDUCTOR
INTEGRATE CIRCUIT, TEST
SUBSTRATE, AND TEST
SUBSTRATE GROUP

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) Group Art Unit: 2123
)
) Examiner: Sharon, Ayal I
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) Confirmation No. 3384
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) Mail Stop AF

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7/27/07

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDMENT AFTER FINAL

In reply to the Final Office Action mailed May 22, 2007, the period for response being on August 22, 2007, and pursuant to 37 C.F.R. § 1.116, Applicants propose that this application be amended as follows:

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks begin on page 7 of this paper.